Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **DNC (1)**
2. **VIN**
3. **TEMP**
4. **GND (2 pads)**
5. **TRIM / NR**
6. **VOUT (2 pads)**
7. **DNC (1)**

**Notes: (1) = Do not connect**

**.068”**

**7**

**6**

**6**

**5**

**1**

**2**

**3**

**4**

**4**

**IC05061**

**MASK**

**REF**

**.034”**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .003” X .003”**

**Backside Potential:**

**Mask Ref: IC05061**

**APPROVED BY: DK DIE SIZE .054 X .034” DATE: 9/8/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: INA271**

**DG 10.1.2**

#### Rev B, 7/19/02